

Application Serial No. : 10/714,031
Filed : 14 November 2003
Applicants : W. Hubis
Title : METHODS AND STRUCTURES FOR A
CACHING TO ROUTER IN ISCSI STORAGE
SYSTEMS
Art Unit : 2144
Examiner : G. Bengzon
Docket Number : 03-1651
Date : 3 March 2008

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR PRE-APPEAL BRIEF REVIEW

Sir:

This request replaces the same request filed earlier today mistakenly without a signature. In response to the Final Office Action mailed 4 January 2008, in conjunction with the Notice of Appeal filed herewith, and in accordance with the procedure outlined in OG Notices (12 July 2005), please consider these remarks.

No amendment is being submitted with this request. This request is filed concurrently with a Notice of Appeal. Applicants hereby request review of the final rejection in the above-identified matter for the reasons stated herein below.

Reasons for Requested Review

**REFERENCES FAIL TO SHOW A ROUTER PROVIDING RECITED
"CACHE" FEATURES - EXAMINER IS APPLYING IMPROPER HINDSIGHT**

First and foremost, nothing in the art of record (considered individually or in any combination) teaches or reasonably suggests an iSCSI router (or any network router device) that includes features for a cache memory as the memory is recited in the rejected claims

The Examiner suggests that Mullendore is sufficient to show a buffer (called a "cache" in Mullendore) and that even if Mullendore, per se, does not teach the recited cache functions (i.e., for satisfying read requests without forwarding a block request through the router) then well known (essentially admitted art) is sufficient for that purpose.

Applicant responds that use of a cache in other contexts to speed read request processing is generally known in the art and is admitted in the Background section of the subject application. For example, processors and storage devices/systems use such caching techniques. However, such caching is not known in the art of network routers and in particular iSCSI routers. Rather, a router's intended purpose is to pass an exchange from a source device to a destination device (generally based on addressing information provided). Network/iSCSI routers do not at present monitor or process the content of such exchanges to determine if an exchange represents a "read" request from a first device to request data from a second device. Only the enhanced router processing of this invention can process the read request from the cache memory without ever forwarding the exchange to the destination device.

As regards independent claim 1, the Examiner points to paragraph 0072 in describing figure 7 of Mullendore as teaching all recited elements. While Applicant admits that Mullendore uses the word "cache" he provides no explanation of its function other than as a buffer to hold data in far-end switch 240 until an addressed far-end target device 245 is ready to accept more data. In other words, Mullendore teaches nothing more than a simple buffer for "speed matching" in the transfers between an initiator 235 and a target 245. Nothing in Mullendore teaches the complexity of a router that processes the block level storage requests exchanged between a first and second iSCSI device coupled through the router. By so processing the block level storage requests, the router of claim 1 may store data blocks in its local cache memory as they are exchanged between the first and second devices. In addition, when the first device issues a read block level storage request, the router may complete the request by returning data blocks from its local cache memory without ever forwarding the storage request to the second device (e.g., without forwarding a read request to the target device.).

Originally filed dependent claim 14 (originally dependent from 11 - now integrated therein) and 20 (originally dependent from 18 - now integrated therein) included similar recitations and were rejected in the first office action (mailed 24 July 2007). There the Examiner rejected claims 14 and 20 under §103 as unpatentable over Mullendore in view of "well-known" prior art making essentially the same argument. Applicant strongly disagreed in the response filed 24 October 2007. The Examiner maintains the same position in this final rejection stating in essence that it would be obvious to combine the standard features of an iSCSI router as taught by Mullendore with the admitted prior art (namely - admitted art that caching functions in other contexts are well known). There is no art provided by the Examiner or any suggestion in the art to apply cache memory management techniques and structures within a network appliance router (a TCP/IP router). As noted, Mullendore suggests nothing more than well-known speed-matching buffering. Though he misuses the word "cache" in reference to his buffer he makes clear that the buffer is used merely to hold data (in far-end switch 240) until the receiving device (target 245) is ready to receive more data - the very essence of a speed-matching buffer. Mullendore suggests nothing more of use of the buffer for cache purposes such as recited in original claims 14 and 20 (now integrated into each independent claim 1, 11, 15, and 18). These caching features in a network appliance router (e.g., a TCP/IP router) are the very essence of the present invention. Thus it is only through improper hindsight applying the teachings of the subject application that the Examiner asserts this "well-known" knowledge.

Conclusion

In view of the above discussion, Applicants assert that all independent claims 1, 11, 15, and 18 are allowable at least for the reasons stated above. At least these same arguments apply to all remaining dependent claims. Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

Applicants have submitted herewith a Notice of Appeal along with the appropriate fees therefore. Applicants believe no further fees are due in this matter. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,

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